CLAIMS

What is Claimed is:

1. A DC-to-DC power converter comprising:

a transformer having a primary winding and at least first and second secondary windings;

an input circuit coupled to said primary winding and adapted to apply an alternating polarity square wave voltage to said primary winding;

an output circuit comprising an output filter coupled to a tap of said first secondary winding, said output filter providing a DC output voltage, a first synchronous rectifier coupled to a first end of said first secondary winding and a second synchronous rectifier coupled to a second end of said first secondary winding, said second secondary winding having a first end coupled to a control terminal of said first synchronous rectifier and a second end coupled to a control terminal of said second synchronous rectifier;

a first snubber circuit coupled between said control terminal of said first synchronous rectifier and said second end of said first secondary winding; and

a second snubber circuit coupled between said control terminal of said second synchronous rectifier and said first end of said first secondary winding;

wherein, said first and second snubber circuits provide faster transition of said first and second synchronous rectifiers, respectively, between on and off states.

2. The power converter of Claim 1, wherein said first and second snubber circuits further comprise respective first and second capacitors.

3. The power converter of Claim 1, wherein first and second synchronous rectifiers comprise respective first and second MOSFET devices.

4. The power converter of Claim 3, wherein said control terminals of said first and second synchronous rectifiers further comprise gate terminals of said first and second MOSFET devices.

5. The power converter of Claim 3, wherein said first end of said first secondary winding is coupled to a drain terminal of said first MOSFET device and said second end of said first secondary winding is coupled to a drain terminal of said second MOSFET device.

6. The power converter of Claim 3, wherein said first and second snubber circuits comprise respective first and second capacitors having capacitances corresponding to a size of said first and second MOSFET devices.

7. The power converter of Claim 1, wherein said input circuit further comprises a full bridge topology.

8. In a DC-to-DC power converter comprising a transformer having a primary winding and at least first and second secondary windings, an input circuit coupled to said primary winding and adapted to apply an alternating polarity square wave voltage to said primary winding, and an output circuit comprising an output filter coupled to a tap of said first secondary winding, said output filter providing a DC output voltage, a first synchronous rectifier coupled to a first end of said first secondary winding and a second synchronous rectifier coupled to a second end of said first secondary winding, said second secondary winding having a first end coupled to a control terminal of said first synchronous rectifier and a second end coupled to a control terminal of said second synchronous rectifier, an improvement comprises:

a first snubber circuit coupled between said control terminal of said first synchronous rectifier and said second end of said first secondary winding; and

a second snubber circuit coupled between said control terminal of said second synchronous rectifier and said first end of said first secondary winding;

wherein, said first and second snubber circuits provide faster transition of said first and second synchronous rectifiers, respectively, between on and off states.

9. The power converter of Claim 8, wherein said first and second snubber circuits further comprise respective first and second capacitors.

10. The power converter of Claim 8, wherein first and second synchronous rectifiers comprise respective first and second MOSFET devices.

11. The power converter of Claim 10, wherein said control terminals of said first and second synchronous rectifiers further comprise gate terminals of said first and second MOSFET devices.

12. The power converter of Claim 10, wherein said first end of said first secondary winding is coupled to a drain terminal of said first MOSFET device and said second end of said first secondary winding is coupled to a drain terminal of said second MOSFET device.

13. The power converter of Claim 10, wherein said first and second snubber circuits comprise respective first and second capacitors having capacitances corresponding to a size of said first and second MOSFET devices.

14. The power converter of Claim 8, wherein said input circuit further comprises a full bridge topology.

15. A method of improving low-load efficiency of an isolated DC-to-DC power converter comprising a transformer having a primary winding and at least first and second secondary windings on which an alternating polarity square wave voltage is applied, and an output circuit comprising an output filter coupled to a tap of said first secondary winding, said output filter providing a DC output voltage, a first synchronous rectifier coupled to a first end of said first secondary winding and a second synchronous rectifier coupled to a second end of said first secondary winding, said second secondary winding having a first end coupled to a control terminal of said first synchronous rectifier and a second end coupled to a control terminal of said second synchronous rectifier, the method comprises:

absorbing charge across said first and second synchronous rectifiers during respective off states of said first and second synchronous rectifiers; and

injecting charge into said control terminals of said first and second synchronous rectifiers during respective on states of said first and second synchronous rectifiers.

16. The method of Claim 15, wherein said absorbing step further comprises charging first and second capacitors coupled to respective ones of said first and second synchronous rectifiers.

17. The method of Claim 16, wherein said injecting step further comprises discharging said first and second capacitors into respective control terminals of said second and first synchronous rectifiers.